What is claimed is:

1. A method for forming a self-aligned gate structure around an emitter tip, comprising:

forming a cathode on a substrate, the cathode having an emitter tip;

forming an insulator layer over the cathode and the emitter tip;

ion etching the insulator layer; and

forming a gate layer on the insulator layer.

2. The method of claim 1, wherein forming a gate layer includes:

depositing a refractory metal on the insulator layer; and

using a chemical mechanical planarization (CMP) process on the refractory metal in order to expose a portion of the insulator layer surrounding the emitter tip.

3. The method of claim 2, wherein the method further includes removing a portion of the insulator layer surrounding the emitter tip in order to uncover the emitter tip.

4. The method of claim 1, wherein ion etching the insulator layer includes using an ion gun as a source of the ions.

5. The method of claim 1, wherein ion etching the insulator layer includes using an Argon plasma ion source.

6. The method of claim 1, wherein ion etching the insulator layer includes using an Oxygen plasma ion source.

7. The method of claim 1, wherein the method further includes coating the emitter tip with a low work function material.

8. The method of claim 1, wherein forming a cathode on a substrate includes forming the cathode on a glass substrate.

9. The method of claim 1, wherein forming a cathode on a substrate includes forming the cathode on a doped silicon material substrate.

10. The method of claim 1, wherein forming a gate layer includes forming a molybdenum (Mo) gate layer.

11. The method of claim 1, wherein forming a gate layer includes forming a tungsten (W) gate layer.

12. The method of claim 1, wherein forming a gate layer includes forming a titanium (Ti) gate layer.

13. A method for forming a self-aligned gate structure around an emitter tip, comprising:

forming a cathode on a substrate, the cathode having an emitter tip;

forming an insulator layer over the cathode and the emitter tip;

ion etching the insulator layer; and

forming a gate layer on the insulator layer, wherein forming a gate layer includes;

depositing a refractory metal on the insulator layer; and

using a chemical mechanical planarization (CMP) process on the refractory metal in order to expose a portion of the insulator layer surrounding the emitter tip.

14. A method for forming a self-aligned gate structure around an emitter tip, comprising:

forming a cathode on a substrate, the cathode having an emitter tip;

forming an insulator layer over the cathode and the emitter tip;

ion etching the insulator layer using an ion gun as a source of the ions; and

forming a gate layer on the insulator layer, wherein forming a gate layer includes;

depositing a refractory metal on the insulator layer; and

using a chemical mechanical planarization (CMP) process on the refractory metal in order to expose a portion of the insulator layer surrounding the emitter tip.

15. A method for forming a self-aligned gate structure around an emitter tip, comprising:

forming a cathode on a substrate, the cathode having an emitter tip;

forming an insulator layer over the cathode and the emitter tip;

ion etching the insulator layer using an Argon plasma ion source; and

forming a gate layer on the insulator layer, wherein forming a gate layer includes;

depositing a refractory metal on the insulator layer; and

using a chemical mechanical planarization (CMP) process on the refractory metal in order to expose a portion of the insulator layer surrounding the emitter tip.

16. A method for forming a self-aligned gate structure around an emitter tip, comprising:

forming a cathode on a glass substrate, the cathode having an emitter tip;

forming an insulator layer over the cathode and the emitter tip;

ion etching the insulator layer using an Argon plasma ion source; and

forming a gate layer on the insulator layer, wherein forming a gate layer includes;

depositing a refractory metal on the insulator layer;

using a chemical mechanical planarization (CMP) process on the refractory metal in order to expose a portion of the insulator layer surrounding the emitter tip;

removing a portion of the insulator layer surrounding the emitter tip in order to uncover the emitter tip; and

coating the emitter tip with a low work function material.

17. A method of forming a field emission device on a substrate, comprising:

forming a cathode emitter tip in a cathode region of the substrate;

forming a gate insulator layer on the emitter tip and the substrate;

using an ion etch process in order to reduce the thickness of the gate insulator layer in the cathode region more rapidly than in the isolation region;

forming a gate on the gate insulator layer; and

forming an anode opposite the emitter tip.

18. The method of claim 17, wherein using an ion etch process to reduce the thickness of the gate insulator layer includes forming a buffer layer on the cathode emitter tip prior to using the ion etch process in order to protect the emitter tip from over etching.

19. The method of claim 18, wherein forming a buffer layer includes forming a dielectric layer of silicon nitride (Si_3N_4).

20. The method of claim 17, wherein forming the cathode emitter tip includes forming a polysilicon cone.

21. The method of claim 17, wherein forming the cathode emitter tip includes forming a metal silicide on a polysilicon cone.

22. The method of claim 17, wherein forming a gate includes:

depositing a conductive material on the gate insulator layer; and

using a chemical mechanical planarization (CMP) process on the conductive material in order to expose a portion of the gate insulator layer surrounding the emitter tip.

23. The method of claim 17, wherein forming a field emitter device on a substrate includes forming the field emitter device on a glass substrate.

24. The method of claim 17, wherein forming a field emitter device on a substrate includes forming the field emitter device on a doped silicon material substrate.

25. The method of claim 17, wherein forming a gate includes forming a gate from a refractory metal.

26. The method of claim 17, wherein forming a gate includes forming a gate from doped polysilicon.

27. A method of forming a field emission device on a substrate, comprising:

forming a cathode emitter tip in a cathode region of the substrate;

forming a gate insulator layer on the emitter tip and the substrate;

using an ion etch process in order to reduce the thickness of the gate insulator layer in the cathode region more rapidly than in the isolation region;

forming a gate on the gate insulator layer, wherein forming a gate includes;

depositing a conductive material on the gate insulator layer; and

using a chemical mechanical planarization (CMP) process on the conductive material in order to expose a portion of the gate insulator layer surrounding the emitter tip; and

forming an anode opposite the emitter tip.

28. The method of claim 27, wherein using an ion etch process to reduce the thickness of the gate insulator layer includes forming a buffer layer on the cathode emitter tip prior to using the ion etch process in order to protect the emitter tip from over etching.

29. The method of claim 28, wherein forming a buffer layer includes forming a dielectric layer of silicon nitride (Si_3N_4).

30. The method of claim 27, wherein forming the cathode emitter tip includes forming a polysilicon cone.

31. The method of claim 27, wherein forming a field emitter device on a substrate includes forming the field emitter device on a glass substrate.

32. The method of claim 27, wherein forming a field emitter device on a substrate includes forming the field emitter device on a doped silicon material substrate.

33. A method of forming a field emission device on a glass substrate, comprising:

forming a cathode emitter tip in a cathode region of the substrate, wherein forming the cathode emitter tip includes forming a polysilicon cone;

forming a gate insulator layer on the emitter tip and the substrate;

using an ion etch process in order to reduce the thickness of the gate insulator layer in the cathode region more rapidly than in the isolation region, wherein the ion etch process further includes;

forming a dielectric layer of silicon nitride (Si_3N_4) on the cathode emitter tip prior to using the ion etch process in order to protect the emitter tip from over etching;

forming a gate on the gate insulator layer, wherein forming a gate includes;

depositing a conductive material on the gate insulator layer; and

using a chemical mechanical planarization (CMP) process on the conductive material in order to expose a portion of the gate insulator layer surrounding the emitter tip; and

forming an anode opposite the emitter tip.

34. The method of claim 33, wherein depositing a conductive material includes depositing a refractory metal.

35. The method of claim 33, wherein depositing a conductive material includes depositing doped polysilicon.

36. A field emitter array, comprising:

a number of cathodes formed in rows along a substrate;

a gate insulator formed along the substrate and surrounding the cathodes;

a number of gate lines formed on the gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a gate insulator layer on the emitter tips and the substrate, wherein forming the gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips.

37. The field emitter array of claim 36, wherein the number of gate lines and the number of cathodes are formed using a self-aligned technique.

38. The field emitter array of claim 36, wherein the number of cathodes include polysilicon cones.

39. The field emitter array of claim 36, wherein the number of cathodes include metal silicides on the polysilicon cones.

40. The field emitter array of claim 36, wherein the substrate includes glass.

41. The field emitter array of claim 36, wherein the number of gate lines include refractory metals.

42. The field emitter array of claim 36, wherein the number of gate lines include doped polysilicon.

~~43. A flat panel display, comprising:~~

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes formed in rows along the substrate;

a gate insulator formed along the substrate and surrounding the cathodes;

a number of gate lines formed on the gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, wherein the anodes include multiple phosphors, and wherein

the intersection of the rows and columns form pixels, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a gate insulator layer on the emitter tips and the substrate, wherein forming the gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips;

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

44. The flat panel display of claim 43, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

45. The flat panel display of claim 43, wherein the number of cathodes include metal silicides on the polysilicon cones.

46. The flat panel display of claim 43, wherein the number of gate lines include refractory metals.